CLOCK GENERATION FOR MULTIPLE SECONDARY BUSES OF A PCI BRIDGE

ABSTRACT OF THE DISCLOSURE

Embodiments are provided in which clock generation for a PCI bridge and its N attached secondary buses is carried out by using an external PLL clock generator which generates N+1 first clock signals at a first frequency to the bridge and to N multiplexers. The bridge in turn generates N second clock signals to the N multiplexers. Each of the N clock signals generated by the bridge can be at either a second or third frequency. Each of the N multiplexers passes one of the first clock signal and second clock signal to a secondary bus depending on the speed of the slowest adapter on the secondary bus.